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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,723	07/31/2001	Cheol Min Ju	P-0231	1248

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	3

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/917,723	Applicant(s) JU, CHEOL MIN	
	Examiner Yolanda Wilson	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1 and 18 recites the limitation "the safeguard area" in each respective claim. There is insufficient antecedent basis for this limitation in the claim. Please change to 'a safeguard area'. There is no indication that 'safeguard area' is located in the claim prior to its use.

3. Claim 10 recites the limitation "the safeguard function area" in each respective claim. There is insufficient antecedent basis for this limitation in the claim. Please change to 'a safeguard function area'. There is no indication that 'safeguard function area' is located in the claim prior to its use.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 6,14, and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 6,14, and 23 contain the subject matter 'the Kernel processes a fault generated in the Kernel area as a simple error'. This subject matter has not been disclosed within the specification of this patent application.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kaplan et al. (USPN US006282657B1). As appears in claims 1 and 18, Kaplan et al. discloses generating a system call; declaring certain functions as a safeguard; verifying a validity of a user buffer using a user buffer address checking function declared as the safeguard; determining whether the user buffer address checking function is declared as the safeguard by calling an exception processor, if the user buffer address area is not valid; identifying an identifier of the safeguard by calling a safeguard exception processor, if the user buffer address checking function is identified as a function in the safeguard area; identifying whether the user buffer address checking function is defined in the system by identifying the safeguard identifier; and returning an error value to the user process if the user buffer address checking function is defined in the system in column 1, lines 46 – column 2, line 3. The safeguard is the address being within the address range, which is the safeguard area. The safeguard identifier is the address value. The exception processor is the flip-flop circuit and the safeguard exception processor is the kernel data fetch supervisor circuit.

8. As per claims 2 and 19, Kaplan et al. discloses returning a success value to the user process, and at the same time, exiting the declared safeguard function if the user memory is valid in column 1, lines 51-56.

9. As per claims 3 and 20, Kaplan et al. discloses exiting the user process if the user buffer address checking function is not defined in the system in column 1, line 61 – column 2, line 3.

10. As per claims 4 and 21, Kaplan et al. discloses wherein the step of verifying the validity of a user buffer comprises: detecting a page within the user buffer; and determining whether a fault is generated by sequential access (read/write) to the address area of the detected page in column 1, lines 46 – column 2, line 3.

11. As per claims 5 and 22, Kaplan et al. discloses wherein the step of verifying the validity of a user buffer further comprises accessing via a Kernel the user buffer address area and verifying the validity of the user buffer in column 1, lines 51-56.

12. As per claims 6 and 23, Kaplan et al. discloses wherein the Kernel processes a fault generated in the Kernel area as a simple error in column 1, line 61 – column 2, line 3.

13. As per claims 7 and 24, Kaplan et al. discloses wherein the Kernel uses a safeguard to process the fault generated in the Kernel area in column 1, lines 51-56.

14. As per claims 8 and 25, Kaplan et al. discloses wherein the step of verifying the validity of a user buffer is performed without using a MMU (Memory Management Unit) Table in column 1, lines 51-56.

15. As per claims 9 and 26, Kaplan et al. discloses wherein each declared safeguard area has a unique identifier in column 1, lines 51-56. The safeguard identifier is the address value.

16. As per claim 10, Kaplan et al. discloses performing a system call; declaring a validity checking function as a safeguard function; identifying whether the validity checking function is declared as the safeguard function by calling an exception processor if the user memory area is not valid; calling a safeguard exception processor; and identifying an identifier of the safeguard exception processor if the validity checking function is in the safeguard function area; recognizing via the safeguard exception processor that a subject of the process is the validity checking function and identifying whether validity checking the function is defined in the system through the identifier of the safeguard function; and processing the validity checking function as defined in the system which performs the process of the function, if the validity checking function is defined in the system in column 1, lines 46 – column 2, line 3. The safeguard is the address being within the address range, which is the safeguard area. The safeguard identifier is the address value. The exception processor is the flip-flop circuit and the safeguard exception processor is the kernel data fetch supervisor circuit.

17. As per claim 11, Kaplan et al. discloses verifying a validity of a user memory area using the validity checking function, wherein the method further comprises returning a success value to the user process, and at the same time, exiting the declared safeguard function, if the user memory area is valid in column 1, lines 51-56.

18. As per claim 12, Kaplan et al. discloses exiting the user process when the validity checking function is not defined in the system in column 1, line 61 – column 2, line 3.

19. As per claim 13, Kaplan et al. discloses Kaplan et al. discloses accessing via a Kernel a user memory area and verifying a validity of the user buffer in column 1, lines 51-56.

20. As per claim 14, Kaplan et al. discloses wherein the Kernel treats a fault generated in the Kernel area as a simple error in column 1, line 61 – column 2, line 3.

21. As per claim 15, Kaplan et al. discloses wherein the Kernel uses the safeguard function in order to process the fault generated in the Kernel area in column 1, lines 51-56.

22. As per claim 16, Kaplan et al. discloses wherein the validity verifying step is executed without using a MMU (Memory Management Unit) Table in column 1, lines 51-56.

23. As per claim 17, Kaplan et al. discloses wherein the declared safeguard area include a unique identifier in column 1, lines 51-56. The safeguard identifier is the address value.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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